REMARKS

The discrepancy between the reference number used on page 4 of the specification and Fig. 1 of the drawings, to identify the manual test circuit, has been remedied by amending page 4 to use the same number used in Fig. 1.

The allowance of original claims 3-4 and 7-8 is acknowledged with appreciation.

Claims 2 and 6 have been canceled.

Claims 1 and 5 have been rejected under 35 U.S.C. 103(a) on the basis of a combination of three references, namely, Howell 4,150,411, Anderson 6,434,715 and Banu 2001/0002123.

Claim 1 requires a microcontroller that is defined as follows:

> a microcontroller receiving said sensor output signal and initiating the generation of a trip signal upon detection of said ground-fault or said grounded-neutral condition in said power distribution system, said microcontroller being programmed to
>
> use said sensor output signal to detect ground-fault conditions during spaced time intervals, and
>
> use said sensor output signal to detect grounded-neutral condition during intervening time intervals between said spaced time intervals.

Claims 1 and 5 both require an analog memory circuit that is defined as providing:

> a timing function to control said spaced time intervals and said intervening time intervals, and
>
> a memory function set in response to detection of a ground-fault or grounded-neutral condition to resume a circuit trip if power is temporarily lost before said circuit interrupter activates.

The circuitry in Fig. 1 that corresponds to the analog memory circuit of claim 1 is identified by the reference numeral 28 in Fig. 1 of the drawings in the present application, reproduced below:

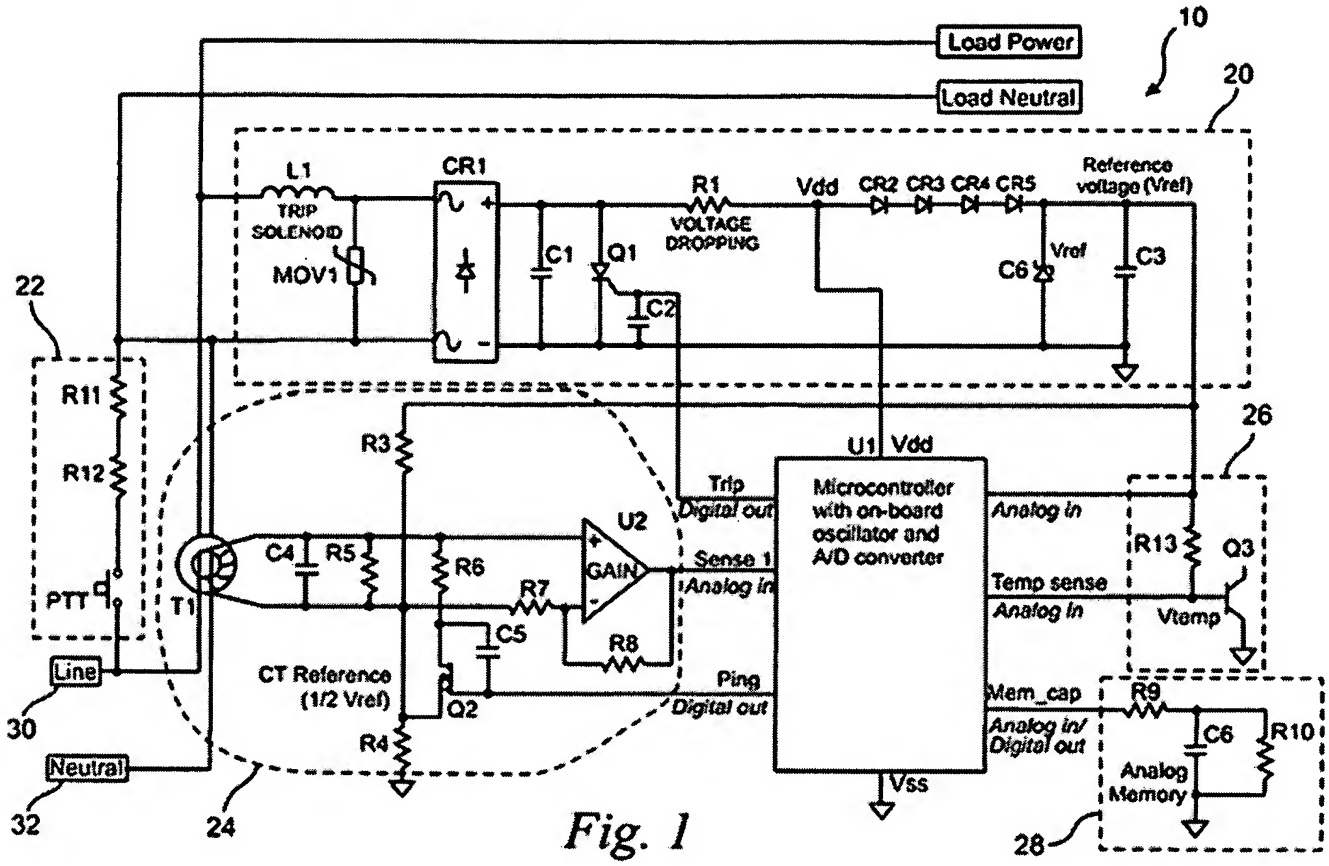


Fig. 1

The circuit 28 in Fig. 1 is described in the specification as follows:

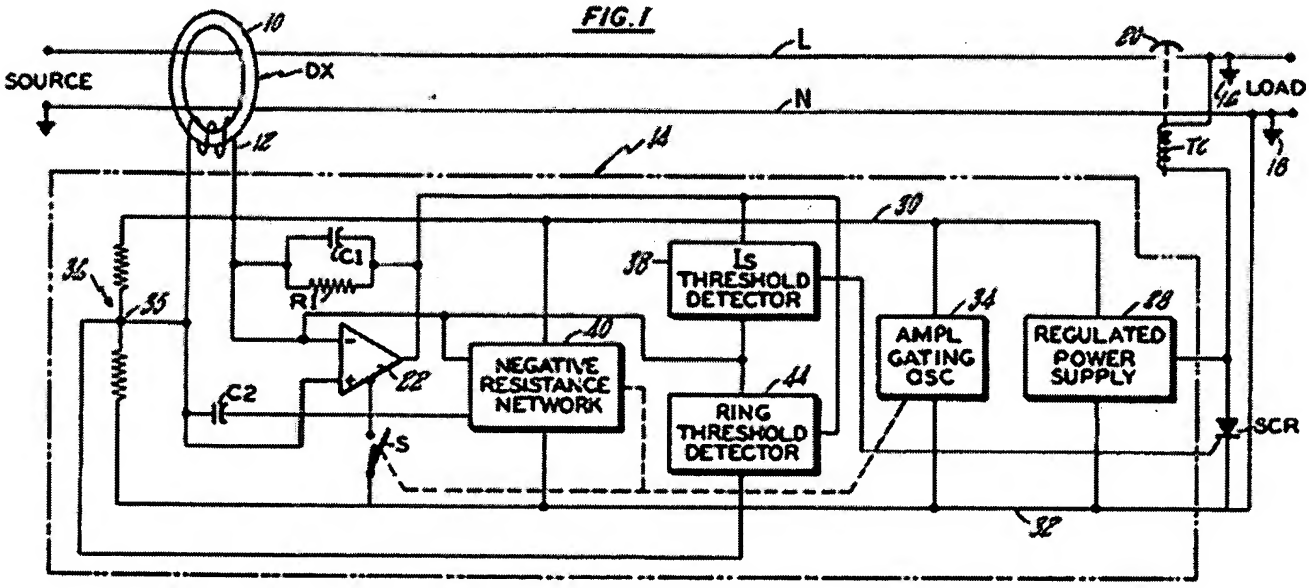
An analog, short-term memory circuit 28 consists of a capacitor C6, a load resistor R9 and a bleed resistor R10. The microcontroller U1 uses a bi-directional pin Mem_cap, as an analog input to read the voltage of the memory circuit 28 and as a digital output to charge the capacitor C6 of the memory circuit 28. If a fault is detected, software running in the microcontroller U1 causes a charge to be placed on the capacitor C6. If power is lost before the trip solenoid is able to open the contacts, the trip memory (i.e., voltage on the capacitor C6) will remain for a short time and cause reactivation of the trip function (by the microcontroller U1) upon resumption of supply voltage. The memory circuit 28 allows the GFCI circuit 10 to operate from a half-wave-rectified or other discontinuous power source.

Referring now to FIG. 2, the timing diagram shows the use of the analog memory circuit 28 during normal operation (no fault detected), for timing purposes to determine when to execute the grounded-neutral and ground-fault

checks. The memory circuit 28 allows the timing of grounded-neutral checks to remain consistent even if a half-wave-rectified (discontinuous) power supply is used. When the voltage of the memory circuit reaches the near-discharged state, the microcontroller U1 charges the capacitor C6 to a voltage level less that the amount required to indicate a pending trip, as discussed above and executes a continuous ground-fault detection mode during the time interval until the voltage capacitor C6 reaches the near-discharged state again. When the voltage of the memory circuit 28, sampled by the microcontroller U1, reaches the near-discharged state, a grounded-neutral check is executed during the intervening time or space interval. This cycle occurs a few times per second as illustrated, and can be adjusted by varying the values of the memory capacitor C6 and the bleed resistor R10.

Application, pp. 8-9.

The Office Action alleges that the relevant portions of the Howell patent are the signal processing circuit 14 and the RC circuit containing resistor R1 and capacitor C1, all of which are shown in Fig. 1 of Howell, reproduced below:



The description of R1 and C1 in the Howell patent is as follows:

> The voltage developed across capacitor C1 as the result of the integration of the amplifier feedback current pulses if over a ground fault or secondary current sampling period is monitored by a Is threshold detector 38. If the voltage developed across capacitor C1 exceeds a predetermined threshold level, signifying a ground fault current of trip level magnitude, detector 38 develops a triggering voltage on the gate of thyristor SCR which then fires to draw sufficient current through trip coil TC to initiate opening of contacts 20, interrupting the distribution circuit. Integrating capacitor C1 is shunted by a large discharge resistor R1, such that a portion of the charge on capacitor C1 may leak off in the intervals between chargings.

Howell, col. 8, ll. 37-50.

The Office Action acknowledges that "Howell does not teach that the signal processor is a microcontroller." The Office Action then attempts to rely on Andersen to overcome this shortcoming of the Howell disclosure. Specifically, the Office Action alleges:

> Anderson teaches a circuit interrupter to protect against fault conditions wherein a microcontroller is used to detect fault currents from a current sensor and to trip the circuit if a fault is detected (column 1 lines 15-28).
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Howell with Anderson, by implementing the threshold detector circuits (38 & 44) of Howell as firmware in a microprocessor as taught by Anderson to receive a sensor output signal from the amplifier (22) and generating a trip signal upon the detection of an over current condition for the purpose of reducing the size and complexity of the circuit.

Office Action, p. 5.

However, if Andersen's microprocessor replaces only the threshold detectors 38 and 44 in the Howell signal processing circuit 14, the Andersen microprocessor will not be performing the functions that applicants' claims 1 and 5 require the microcontroller to perform, namely:

> . . . said microcontroller being programmed to
>
> use said sensor output signal to detect ground-fault conditions during spaced time intervals, and
>
> use said sensor output signal to detect grounded-neutral condition during intervening time intervals between said spaced time intervals.

Specifically, Howell's threshold detectors 38 and 44 have nothing to do with "spaced time intervals" or "intervening time intervals," which are explicitly required by the language of claims 1 and 5. Thus, the hypothetical combination of Howell and Andersen cannot yield the invention defined by applicants' claims 1 and 5.

The Office Action also acknowledges that "Howell further does not teach that the analog memory circuit provides a timing function to control said spaced time intervals and said intervening time intervals." This is an explicit part of the definition of the analog memory circuit in applicants' claims 1 and 5, and it is not met by the disclosure in the Howell patent. The Office Action attempts to rely on Banu to overcome this shortcoming of the Howell disclosure, alleging:

> Banu et al. teaches a sampling device wherein an analog memory (20) is used to control the timing of the sampling period (paragraph 0010).
>
> It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Howell with Banu et al., by replacing the sampling circuit of Howell (S & 34) with the sampling circuit of Banu by sampling the sensor output signal between the amplifier (22) and capacitor (C1) using an analog memory contained in the analog memory circuit, to control said spaced time intervals and said intervening time intervals of Howell, for the purpose of providing a simple sampling device that reduces aliasing errors.

Office Action, p.4.

However, the "replacement" proposed in the Office Action again would not yield a system that meets the requirements of applicants' claims 1 and 5. Specifically, the hypothetical replacement postulated in the Office Action would not produce a system in which the same analog memory circuit performs the dual functions recited in the last two sub-paragraphs of claim 1. Howell's switch S and oscillator 34 would be replaced with Banu's sampling circuit 10 (including the time delay device 20 that Banu says "can be realized by an analog memory element"), but Howell's capacitor C1 would remain. In fact, the Office Action specifically states that the Banu sampling circuit would sample the signal between the amplifier 22 and the **capacitor C1**. Also, the Office Action identifies Howell's capacitor C1 as performing the function of resuming a circuit trip if power is temporarily lost. Thus, the resulting circuit would have two different analog memory circuits, namely, Howell's circuit that includes capacitor C1 and resistor R1, and Banu's sampling

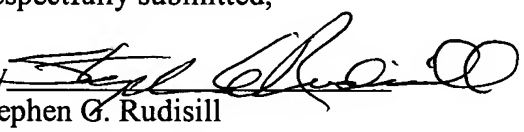
circuit 10 that includes the time delay device 20 (e.g., an analog memory element). This would not satisfy the requirement of claims 1 and 5 that a single analog memory circuit perform the dual functions recited in the last two sub-paragraphs of claims 1 and 5.

To make it clear that the two functions recited in the last two sub-paragraphs of applicants' claims 1 and 5 are both effected by the same analog memory circuit, claims 1 and 5 have been amended to recite "a single analog memory circuit."

It is respectfully requested that the rejection of claims 1 and 5 be reconsidered in light of the above remarks.

Dated: September 29, 2006

Respectfully submitted,

By 

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